In the Claims:

1. (Currently amended) A method of forming a plurality of channel regions ~~channel region~~ between isolation regions of an integrated circuit substrate, the method comprising:

forming a mask on the isolation region that extends onto a portion of the substrate adjacent to the isolation region to provide a shielded portion of the substrate adjacent to the isolation region and an exposed portion of the substrate spaced apart from the isolation region having the shielded portion therebetween, the exposed portion of the substrate comprising a first portion where a gate electrode will be subsequently formed and a second portion where a bit line contact will be subsequently formed, the mask exposing only the first and second portions;

implanting ions into the exposed portion of the substrate using the mask as an implant mask, thereby forming ~~a channel~~ an implant region in only the first and second portions to adjust the threshold voltage of a transistor;

forming a plurality of gate electrodes on the ~~channel~~ implant region; and

implanting ions using the plurality of gate electrodes as an implant mask to form source/drain regions associated with the plurality of gate electrodes and to define separate channel regions ~~between adjacent isolation regions associated with the plurality of gate electrodes~~ from the ~~channel~~ implant region ~~that~~, wherein the separate channel regions are self-aligned to the plurality of gate electrodes.

2. (Previously presented) A method according to Claim 1 wherein the forming the channel region comprises:

implanting a first concentration of ions in the shielded region adjacent to the isolation region; and

wherein the implanting ions comprises implanting a second concentration of ions in the channel region spaced apart from the isolation region, wherein the second concentration is greater than the first concentration.

3. (Previously presented) A method according to Claim 1 wherein the forming a channel region comprises implanting boron ions in the exposed portion.

Claims 4-16 (Canceled).

17. (Previously presented) A method according to Claim 1 wherein at least one of the source/drain regions is in the exposed portion.

18. (Previously presented) A method according to Claim 1 wherein the implanting ions comprises:

implanting first ions of first conductive type; and

implanting second ions of second conductive type.

19. (Previously presented) A method according to Claim 18 wherein the implanting first ions and second ions comprises:

implanting boron ions to provide a first concentration of ions of about 1 x 10^{17} ions/cm^3.

20. (Previously presented) A method according to Claim 1 wherein the source/drain regions comprise lightly doped source/drain structures.

21. (Currently amended) A method of forming a ~~channel region~~ plurality of channel regions between isolation regions of an integrated circuit substrate, the method comprising:

forming a mask on first and second adjacent isolation regions in an integrated circuit substrate and extending onto an active area between the first and second adjacent isolation regions to define first and second shielded portions of the substrate adjacent to the first and second isolation regions and an exposed portion of the substrate therebetween, the exposed portion of the substrate comprising a first portion where a gate electrode will be subsequently formed and a second portion where a bit line contact will be subsequently formed, the mask exposing only the first and second portions;

implanting ions into the exposed portion of the substrate using the mask as an implant mask, thereby forming a single ~~channel~~ implant region in only the first and second portions to adjust the threshold voltage of a transistor;

forming a plurality of gate electrodes on the single ~~channel~~ implant region; and

implanting ions using the plurality of gate electrodes as an implant mask to form source/drain regions associated with the plurality of gate electrodes and to form first and second spaced apart channel regions ~~between adjacent isolation regions associated with the plurality of gate electrodes~~ from the single ~~channel~~ implant region.

22. (Previously presented) A method according to Claim 21 wherein the implanting ions comprises implanting ions to form the first and second spaced apart channel regions self-aligned to the plurality of gate electrodes.

23. (Previously presented) A method according to Claim 21 wherein forming a single channel region comprises implanting boron ions in the exposed portion.

24. (Currently amended) A method of forming a plurality of channel regions ~~channel region~~ between isolation regions of an integrated circuit substrate, the method comprising:

forming a mask on the isolation region that extends onto a portion of the substrate adjacent to the isolation region to provide a shielded portion of the substrate adjacent to the isolation region and an exposed portion of the substrate spaced apart from the isolation region having the shielded portion therebetween;

implanting ions into the exposed portion of the substrate using the mask as an implant mask, thereby forming ~~a channel~~ an implant region in the exposed portion of the substrate to adjust the threshold voltage of a transistor; then

forming a plurality of gate electrodes on the ~~channel~~ implant region; and

implanting ions using the plurality of gate electrodes as an implant mask to form source/drain regions associated with the plurality of gate electrodes and to define separate channel regions ~~between adjacent isolation regions associated with the~~

~~plurality of gate electrodes~~ from the ~~channel~~ implant region, wherein the separate channel regions ~~that~~ are self-aligned to the plurality of gate electrodes.